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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/886,741	06/21/2001	Vincent Chan	ATI.0100680	6028

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EXAMINER	
CHU, CHRIS C	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/886,741	CHAN ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2 - 14, 16 - 20, 22 - 40, 44 - 48 and 50 - 59* is/are pending in the application.

4a) Of the above claim(s) *See Continuation Sheet* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2 - 6, 8, 9, 11, 16 - 18, 20, 23, 44 - 47, 53, 54 and 56 - 59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Continuation of Disposition of Claims: Claims withdrawn from consideration are 7, 10, 12 - 14, 19, 22, 24 - 40, 48, 50 - 52 and 55.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on August 7, 2003 has been received and entered in the case.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 5, 6, 8, 9, 44, 46, 47, 56 and 58 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanioka.

Regarding claim 56, Tanioka discloses in Figs. 2A ~ 2C a device comprising:

- a package module (a structure in Fig. 2A) including a substrate (19) having a standard package footprint;
- an unpackaged semiconductor die (2) directly attached to the package module, the unpackaged semiconductor die encapsulated (16) onto the package module in a structure having a planar top surface; and

- a packaged semiconductor die (17) having a top surface and attached to the package module;
- wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate.

Regarding claim 5, Tanioka discloses in Fig. 2A a plurality of packaged semiconductors (17) being attached to the package module.

Regarding claim 6, Tanioka discloses in Fig. 2A the unpackaged semiconductor die (2) being wire (15) bonded to the package module.

Regarding claim 8, the phrase "wherein attached includes surface-mount technology reflow" is product-by-process limitation. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 9, Tanioka discloses in Fig. 2A the encapsulated structure (2) having a footprint greater than the footprint of the unpackaged semiconductor die (17).

Regarding claim 58, Tanioka discloses in Figs. 2A ~ 2C a multi-die module, comprising:

- a substrate (19) having a first surface and a second surface;
- an unpackaged semiconductor die (2) mounted to the first surface of the substrate, the semiconductor die encapsulated (16) in a structure having a planar top surface; and
- a packaged semiconductor die (17) having a top surface and mounted on the first surface of the substrate;
- wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate.

Regarding claim 44, Tanioka discloses in Fig. 2A further including a second packaged semiconductor die mounted on the first surface of the substrate.

Regarding claim 46, Tanioka discloses in Fig. 2A the unpackaged semiconductor die being mounted to the first surface of the substrate by wire (15) bonding.

Regarding claim 47, Tanioka discloses in Fig. 2A and column 1, line 43 the encapsulating structure (16) being further comprised of an encapsulating material including epoxy, metal cap or silicon coatings.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 16 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanioka in view of Fallon et al.

Regarding claims 2 and 16, Tanioka discloses the semiconductor package set forth in the claims except for the packaged semiconductor being packaged in a ball grid array package. However, Fallon et al. discloses in Fig. 46 a packaged semiconductor (862) being packaged in a ball grid array package. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Tanioka by using the ball grid array package for the packaged semiconductor as taught by Fallon et al. The ordinary artisan would have been motivated to modify Tanioka in the manner described above for at least the purpose of increasing a bond strength between the packaged semiconductor and the substrate.

Regarding claim 45, Tanioka discloses the semiconductor package set forth in the claims except for a plurality of unpackaged semiconductor die mounted on the first surface of the substrate. However, Fallon et al. discloses in column 37, lines 48 and 49 a plurality of unpackaged semiconductor die mounted on the first surface of the substrate. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Tanioka by using the plurality of unpackaged semiconductor die as taught by Fallon et al. The ordinary artisan would have been motivated to modify Tanioka in the manner described above for at least the purpose of increasing power and speed of the module.

6. Claims 3, 4, 17, 18, 20, 53, 54 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanioka in view of Hannah.

Regarding claims 3 and 53, Tanioka discloses the semiconductor die to be graphics-processor. However, Hannah teaches in column 3, lines 42 ~ 46 a semiconductor die to be graphics-processor. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Tanioka by using the graphics-processor for the semiconductor die as taught by Hannah. The ordinary artisan would have been motivated to modify Tanioka in the manner described above for at least the purpose of receiving commands and graphics data from the main CPU of the computer (column 3, lines 42 ~ 46).

Regarding claims 4 and 54, Tanioka discloses the semiconductor die to be memory. However, Hannah teaches in column 5, lines 16 ~ 21 a semiconductor die to be memory. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Tanioka by using the semiconductor die to be memory as taught by Hannah. The ordinary artisan would have been motivated to modify Tanioka in the manner described above for at least the purpose of decreasing a cost (column 5, lines 19 ~ 21).

Regarding claim 57, Tanioka discloses in Figs. 2A ~ 2C a device comprising:

- a package module (a structure at Fig. 2A);
- a die (2) directly attached to the package module, the die encapsulated (16) on the package module in a structure having a planar top surface; and
- a packaged die (17) having a top surface and attached to the package module;

- wherein the planar top surface of the encapsulated structure and the top surface of the packaged memory die are of equal distance from the package module.

Further, the phrase "sized to be interchangeable with standard package sizes" is intended use language which does not differentiate the claimed apparatus over Tanioka.

Tanioka discloses the semiconductor die to be graphics-processor and memory. However, Hannah teaches in column 3, lines 42 ~ 46 and column 5, lines 16 ~ 21 a semiconductor die to be graphics-processor. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Tanioka by using the semiconductor die to be graphics-processor and memory as taught by Hannah. The ordinary artisan would have been motivated to modify Tanioka in the manner described above for at least the purpose of receiving commands and graphics data from the main CPU of the computer (column 3, lines 42 ~ 46).

Regarding claim 17, Tanioka, as modified, discloses a plurality of packaged memory (17) being attached to the package module.

Regarding claim 18, Tanioka, as modified, discloses directly attached including the graphics processing die (2) being wire (15) bonded to the package module.

Regarding claim 20, the phrase "wherein attached includes surface-mount technology reflow" is product-by-process limitation. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to

the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanioka in view of Takano et al.

Regarding claim 11, Tanioka discloses the semiconductor package set forth in the claims except for the standard package sizes being 40mm X 40mm. However, Takano et al. discloses in TABLE 1 a standard package sizes being 40mm X 40mm. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Tanioka by using the standard package sizes as taught by Takano et al. The ordinary artisan would have been motivated to modify Tanioka in the manner described above for at least the purpose of reducing a limitation in the size of a semiconductor chip (column 2, lines 6 and 7).

8. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanioka and Hannah as applied to claim 57 above, and further in view of Takano et al.

Regarding claim 23, Tanioka discloses the semiconductor package set forth in the claims except for the standard package sizes being 40mm X 40mm. However, Takano et al. discloses in TABLE 1 a standard package sizes being 40mm X 40mm. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Tanioka by using the standard package sizes as taught by Takano et al. The ordinary artisan would have been motivated to further modify Tanioka in the manner described above for at least the purpose of reducing a limitation in the size of a semiconductor chip (column 2, lines 6 and 7).

9. Claim 59 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanioka in view of Distefano.

Regarding claim 59, Tanioka discloses in Figs. 2A ~ 2C a multi-die module, comprising:

- a substrate (19) having a first surface;
- an unpackaged semiconductor die (2) mounted to the first surface of the substrate, the semiconductor die encapsulated (16) in a structure; and
- a packaged semiconductor die (17) mounted on the first surface of the substrate.

Tanioka does not disclose the encapsulating structure being further comprised of an encapsulating material of a metal cap. However, Distefano discloses in Fig. 2 and column 4, line 21 ~ 33 an encapsulating structure being further comprised of an encapsulating material of a metal cap (20). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Tanioka by using the metal cap as taught by Distefano. The ordinary artisan would have been motivated to modify Tanioka in the manner described above for at least the purpose of providing a thermal spreader (column 1, lines 45 ~ 50).

Response to Arguments

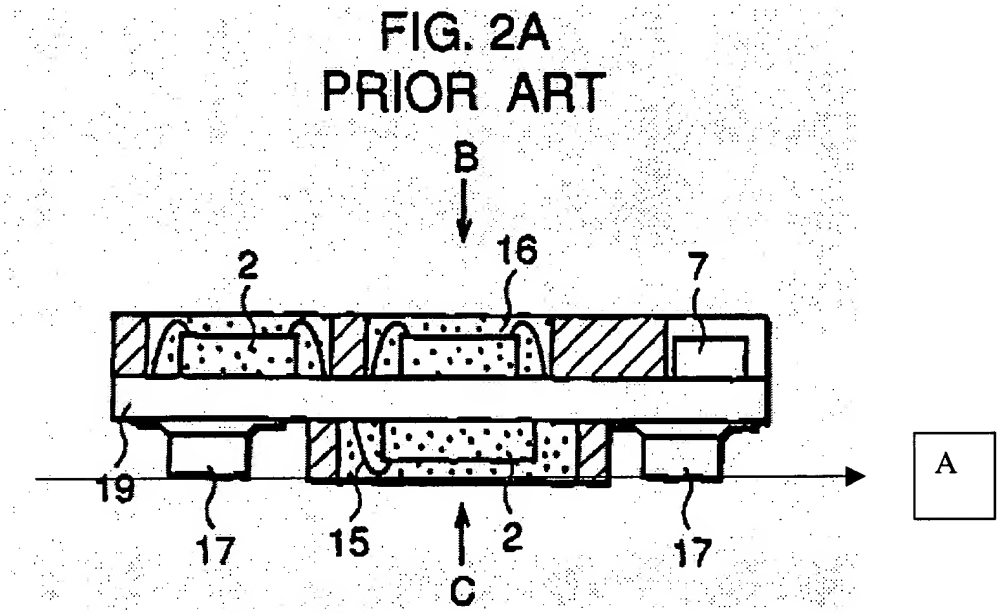
10. Applicant's arguments filed on August 7, 2003 have been fully considered but they are not persuasive.

On page 9, applicant argues "applicants submit that the encapsulation design of Tanioka lacks the advantages presents in Applicant's claimed subject matter." Since applicant merely argues the advantages presents in Applicant's claimed subject matter rather than pointing out specific structural differences, the argument is not persuasive.

Further, applicant argues "the silicon layer 9 interposed between the carrier board 3 and the MCM board 1 as taught by Tanioka is less desirable than Applicants' claimed subject matter as such material is no metal and therefore does not provide the metallic properties such as heat transfer provided by Applicants' claimed subject matter, nor is such material a metal cap as acknowledge in the Office action." Since applicant does not specifically claimed above statement (i.e., the metallic properties such as heat transfer) in the rejected claims, this argument is not persuasive.

Furthermore, applicant argues "applicants submit that nowhere in the Office Action does the Examiner specifically point out where the references recites the claim limitation 'wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate.' ... Applicant submit that Tanioka

does not disclose Applicants' claimed subject matter." This argument is not persuasive. Tanioka clearly shows in Fig. 2A the planar top surface of the encapsulated structure (2) and the top surface of the packaged semiconductor die (17) are of equal distance from the substrate (look at the line A).



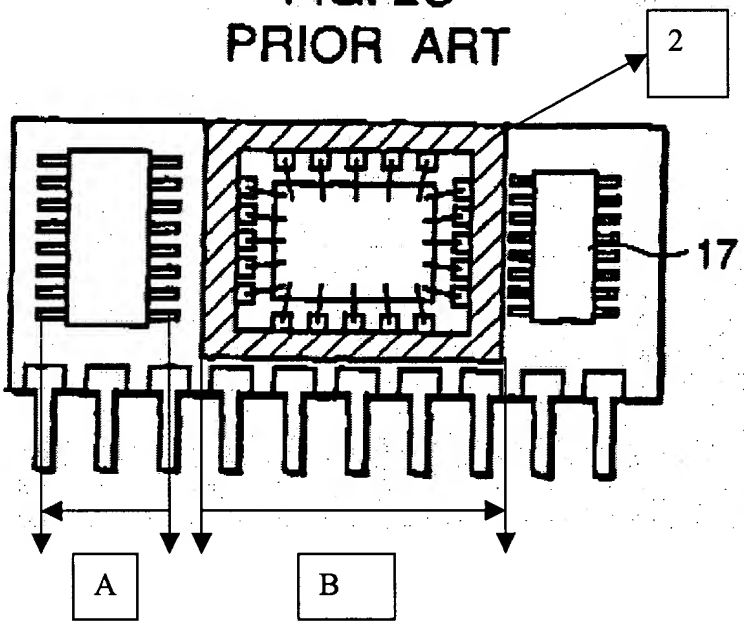
Next, applicant argues "Tanioka does not disclose, teach or suggest, claim 57's language including, inter alia, '... a ... graphics-processing die encapsulated on the package module in a structure having a planar top surface; and a packaged memory die having a top surface and attached to the package module; wherein the planar top surface of the encapsulated structure and the top surface of the packaged memory die are of equal distance from the substrate.,' nor does Tanioka disclose, teach or suggest the subject matter of claim 57 as a whole." This argument is not persuasive. Tanioka clearly shows in Fig. 2A the planar top surface of the encapsulated structure (2) and the top surface of the packaged semiconductor die (17) are of equal distance from the substrate (look at the line A in the previous page).

Next, applicant argues "the Office action asserts that the semiconductor module 'sized to be interchangeable with standard package sizes' employs intended use language. Nevertheless, the claim language 'a package module sized to be interchangeable with standard package sizes' (see M.P.E.P. 2173(b)) is sufficiently accurate, and therefore, the rejection is improper." This argument is not persuasive because the intended use of the claimed invention must result in a structural difference between the claimed invention and Tanioka in order to patentably distinguish the claimed invention from Tanioka. Since Tanioka's package module is capable of performing the intended use language, Tanioka meets the claim.

Next, applicant argues "Tanioka does not disclose, teach or suggest, claim 58's language including, inter alia, '... a an unpackaged semiconductor die ... encapsulated in a structure having a planar top surface; and a packaged semiconductor die having a top surface and mounted on the first surface of the substrate; wherein the planar top surface of the encapsulated structure and the top surface of the packaged memory die are of equal distance from the substrate.,' nor does Tanioka disclose, teach or suggest the subject matter of claim 58 as a whole." This argument is not persuasive. Tanioka clearly shows in Fig. 2A the planar top surface of the a an unpackaged semiconductor die (2) ... encapsulated in a structure having a planar top surface; and a packaged semiconductor die (17) having a top surface and mounted on the first surface of the substrate (19); wherein the planar top surface of the encapsulated structure and the top surface of the packaged memory die are of equal distance from the substrate (look at the line A in the previous page).

Next, applicant argues "Tanioka does not disclose, teach or suggest, either explicitly or implicitly, Applicants claimed, inter alia, wherein the encapsulated structure has a footprint greater than the footprint of the unpackaged semiconductor die." This argument is not persuasive. Tanioka clearly discloses in Fig. 2A and Fig. 2C the encapsulated structure (2) having a footprint (B, see next page) greater than the footprint (A) of the unpackaged semiconductor die (17).

FIG. 2C
PRIOR ART



Next, in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir.

1992). Contrary to applicant's assertion and as stated in previous rejection which is mailed on April 29, 2003, motivation was established by in the knowledge generally available to one of ordinary skill in the art that the ball grid array package increases bond strength between the packaged semiconductor and the substrate.

Next, applicant states "no reference to a patent number could be found in the Office Actions referring to Takano, and further, no reference to a patent to Takano could be found in the attached PTO-892 form entitled "Notice of References Cited." This statement is not true. Takano is found in the attached PTO-892 form entitled "Notice of References Cited" which is mailed on August 14, 2002. Therefore, the rejection is maintained.

Next, applicant argues "neither Tanioka nor Distefano either in combination nor individually disclose, teach or suggest, claim 59's language including, inter alia, '... an unpackaged semiconductor die ... encapsulated in a structure; and a packaged semiconductor die mounted on the first surface of the substrate wherein the encapsulating structure is further comprised of an encapsulating material of a metal cap.' Further, Tanioka and Distefano either in combination or individually fail to disclose, teach or suggest the subject matter of claim 59 as a whole." This argument is not persuasive. Tanioka and Distefano disclose in Fig. 2A an unpackaged semiconductor die (2) ... encapsulated in a structure; and a packaged semiconductor die (17) mounted on the first surface of the substrate wherein the encapsulating structure is further comprised of an encapsulating material of a metal cap (see paragraph seven of this Office action).

Finally, in response to applicant's argument that flanges on the metal cap of the encapsulating material would impermissibly interfere with the unpackaged semiconductor and therefore increase the surface area of the module, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

For the above reasons, the rejection is maintained.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
10/20/03 11:15:23 AM

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
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